Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (Cancelled)
Claim 2 (Cancelled)
Claim 3 (Cancelled)
Claim 4 (Cancelled)
Claim 5 (Cancelled)
Claim 6 (Cancelled)
Claim 7 (Cancelled)
Claim 8 (Cancelled)
Claim 9 (Cancelled)
Claim 10 (Cancelled)
Claim 11 (Cancelled)
Claim 12 (Cancelled)
Claim 13 (Cancelled)
Claim 14 (Cancelled)
Claim 15 (Cancelled)
Claim 16 (Cancelled)
Claim 17 (Cancelled)
Claim 18 (Cancelled)

Claim 19 (Original)

A method of signal demodulation for a circuit having a differential transconductance input cell consisting of separate positive and negative channels for receiving positive and negative channels of said input signal x(t) and amplifying said positive and negative channels of said input signal x(t); a first differential mixer for receiving said amplified input signal x(t), and mixing said input signal x(t) with a first mixing signal $\phi 1$, to generate an output signal $\phi 1$ x(t); a second differential mixer for receiving said signal $\phi 1$ x(t) as an input, and mixing said signal $\phi 1$ x(t) with a second mixing signal $\phi 2$, to generate an output signal $\phi 1$ $\phi 2$ x(t); a pair of current sources Ia and Ib for providing current to respective ones of said positive and negative

channels of said differential transconductance input cell, to reduce the drawn from said first differential mixer; said current sources Ia and Ib being trimmed in a complementary manner where Ia=I+ΔI, and Ib=I-ΔI; said method comprising the steps of:

injecting a two-tone signal at said input;

measuring IM2 at the baseband output of said circuit;

determining the level of ΔI which minimizes IM2;

recording the level of ΔI which minimizes IM2; and

using said recorded level of ΔI during normal operation of said down-convertor.

Claim 20 (Currently Amended)

A method of down-converting a differential input signal x(t) comprising the steps of:

amplifying positive and negative channels of said input signal x(t) using a differential transconductance input cell consisting of separate positive and negative channels;

mixing said amplified input signal x(t) with a first mixing signal ϕ1, to generate an output signal ϕ1 x(t), using a first differential mixer;

mixing said signal ϕ1 x(t) with a second mixing signal ϕ2, to generate an output signal ϕ1 ϕ2 x(t), using a second differential mixer; and

providing current to respective ones of said positive and negative channels of said differential transconductance input cell, using a pair of current sources Ia and Ib, reducing the current drawn from said first differential mixer; and trimming said current sources Ia and Ib in a complementary manner where Ia=I+ΔI, and Ib=I-ΔI; wherein ~~A1~~ ΔI can be manipulated to reduce the IM2 and DC offset in the output signal ϕ1 ϕ2 x(t), and wherein matching parameters for said mixers can be relaxed.

Claim 21 (Previously Presented)
A computer readable memory medium for storing software code executable to perform the method steps of claim 19.

Claim 22 (New)
The method of claim 19, including operating a means for manipulating ΔI to reduce the IM2 and DC offset in the output signal $\phi 1$ $\phi 2$ x(t), whereby matching parameters for said mixers can be relaxed.

Claim 23 (New)
The method of claim 19, including operating a means for setting a level of ΔI.

Claim 24 (New)
The method of claim 19, wherein the current sources Ia and Ib each include parallel arrays of transistors, and the step of using includes selectively driving the parallel arrays of transistors with a level of ΔI.

Claim 25 (New)
The method of claim 20, wherein ΔI is determined using a two-tone test, ΔI being the current level which minimizes IM2 output at baseband.

Claim 26 (New)
The method of claim 25, wherein the two-tone test includes

injecting a two-tone signal as the input signal x(t);

measuring IM2 of the output signal $\phi 1$ $\phi 2$ x(t);

determining the level of ΔI which minimizes IM2;

recording the level of ΔI which minimizes IM2; and

using said recorded level of ΔI during the step of providing current.

Claim 27 (New)

The method of claim 20, wherein the current sources Ia and Ib each include parallel arrays of transistors, and the step of providing current includes selectively driving the parallel arrays of transistors with a level of ΔI.